WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a differential sense amplifier connected to a bit line; and

a data transfer circuit including a column selection switch for turning ON/OFF connection between a data line and the bit line, wherein:

the differential sense amplifier includes a power supply and a transistor array of at least one MOS transistor connecting the power supply with the bit line; and

an on-state resistance of the column selection switch is higher than that of the transistor array.

2. The semiconductor device of claim 1, wherein:

the bit line includes a first bit line and a second bit line that go high and low, respectively, when the differential sense amplifier is activated in a read operation;

the differential sense amplifier includes a P-channel MOS transistor connecting the power supply with the second bit line; and

a potential of the first bit line is higher than a threshold of the P-channel MOS transistor.

3. A semiconductor device, comprising:

a differential sense amplifier connected to a bit line; and

a data transfer circuit including a column selection switch for turning ON/OFF connection between a data line and the bit line,

wherein the column selection switch includes a read column selection switch and a write column selection switch.

4. The semiconductor device of claim 3, wherein an on-state resistance of the read column selection switch is higher than that of the write column selection switch.

5. The semiconductor device of claim 3, wherein the read column selection switch and the write column selection switch are connected to the data line via a common

impurity diffusion layer.

6. The semiconductor device of claim 3, wherein:

the read column selection switch and the write column selection switch along one of a pair of columns adjacent to each other are connected to the same data line as the read column selection switch and the write column selection switch, respectively, along the other one of the pair of columns; and

a pair of the read column selection switches for the pair of columns are connected to the same data line via a common impurity diffusion layer, and a pair of the write column selection switches for the pair of columns are connected to the same data line via a common impurity diffusion layer.

7. A semiconductor device, comprising:

a differential sense amplifier connected to a bit line;

a data transfer circuit including a column selection switch for turning ON/OFF connection between a data line and the bit line; and

a capacitance control switch for turning ON/OFF connection between an additional capacitor and the bit line,

wherein the additional capacitor and the bit line are connected to each other by the capacitance control switch after the differential sense amplifier is activated in a read operation and before the data line and the bit line are connected to each other by the column selection switch.

8. A semiconductor device, comprising:

a differential sense amplifier connected to a bit line;

a data transfer circuit including a column selection switch for turning ON/OFF connection between a data line and the bit line; and

a data line dividing switch for selectively dividing or not dividing the data line,

wherein the data line is divided by the data line dividing switch until the

differential sense amplifier is activated in a read operation and the data line and the bit line are connected to each other by the column selection switch.